NUP1301ML3T1

Low Capacitance Diode Array for ESD Protection in a Single Data Line

NUP1301ML3T1 is a MicroIntegration™ device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (0.9 pF Maximum)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
  - Machine Model = Class C
  - Human Body Model = Class 3B
- Protection for IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- Pb−Free Package is Available

Applications

- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I^2C Bus Protection

MAXIMUM RATINGS (Each Diode) (T_J = 25°C unless otherwise noted)

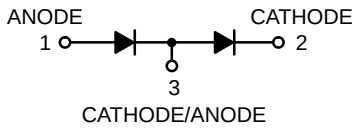
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	70	Vdc
Forward Current	I_F	215	mAdc
Peak Forward Surge Current	$I_{FM(surge)}$	500	mAdc
Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	$I_{F(AV)}$	715	mA
Repetitive Peak Forward Current	I_{FRM}	450	mA
Non−Repetitive Peak Forward Current t = 1.0 μs t = 1.0 ms t = 1.0 S	I_{FSM}	 2.0 1.0 0.5	A

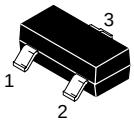
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

ON Semiconductor®

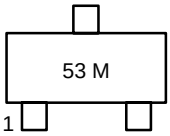
http://onsemi.com





SOT−23
CASE 318
STYLE 11

MARKING DIAGRAM



53 = Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NUP1301ML3T1	SOT−23	3000 / Tape & Reel
NUP1301ML3T1G	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	625	°C/W
Lead Solder Temperature Maximum 10 Seconds Duration	T_L	260	°C
Junction Temperature	T_J	−65 to 150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Reverse Breakdown Voltage ($I_{(BR)}$ = 100 μA)	$V_{(BR)}$	70	−	−	Vdc
Reverse Voltage Leakage Current (V_R = 70 Vdc) (V_R = 25 Vdc, T_J = 150°C) (V_R = 70 Vdc, T_J = 150°C)	I_R	− − −	− − −	2.5 30 50	μAdc
Diode Capacitance (between I/O and ground) (V_R = 0, f = 1.0 MHz)	C_D	−	−	0.9	pF
Forward Voltage (I_F = 1.0 mAdc) (I_F = 10 mAdc) (I_F = 50 mAdc) (I_F = 150 mAdc)	V_F	− − − −	− − − −	715 855 1000 1250	mV_{dc}

2. FR−5 = 1.0 × 0.75 × 0.062 in.
3. Alumina = 0.4 × 0.3 × 0.024 in, 99.5% alumina.

Figure 1. ESD Test Circuit

APPLICATION NOTE

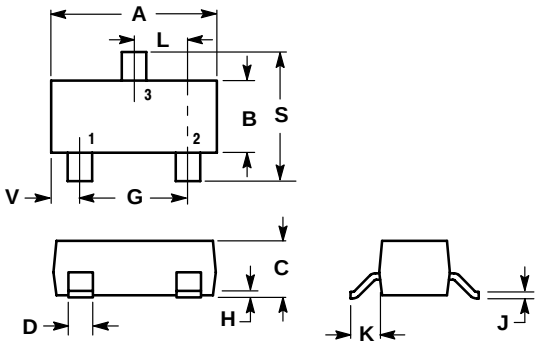
Electrostatic Discharge

A common means of protecting high−speed data lines is to employ low−capacitance diode arrays in a rail−to−rail configuration. Two devices per line are connected between two fixed voltage references such as V_{CC} and ground. When the transient voltage exceeds the forward voltage (V_F) drop of the diode plus the reference voltage, the diodes direct the surge to the supply rail or ground. This method has several advantages including low loading capacitance, fast response time, and inherent bidirectionality (within the reference voltages). See Figure 1 for the test circuit used to verify the ESD rating for this device.

NUP1301ML3T1

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AK

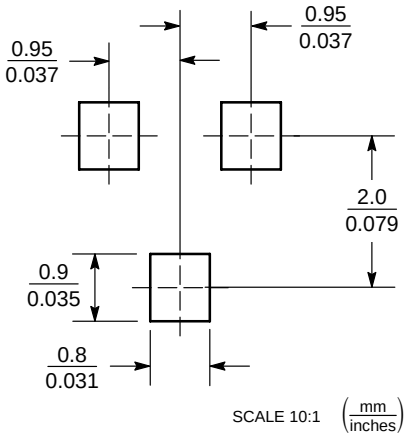


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MicroIntegration is a trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.